正基科技股份有限公司

AMPAK Technology Inc.

AP6398S

Evaluation Board User Manual

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Revision

Revision	Date	Description	Revised By
1.0	2021/ 06 / 22	Initial released	Ali

Contents

1. EVB Introduction

AP6398S2 Evaluation board (EVB) likes as figure1. That is designed for IEEE802.11 a/b/g/n/ac WLAN with integrated Bluetooth application. It is subject to provide a convenient environment for customer's verification on WiFi or Bluetooth function. There are many controller pins and reserved GPIO on Evaluation board which describes as below.

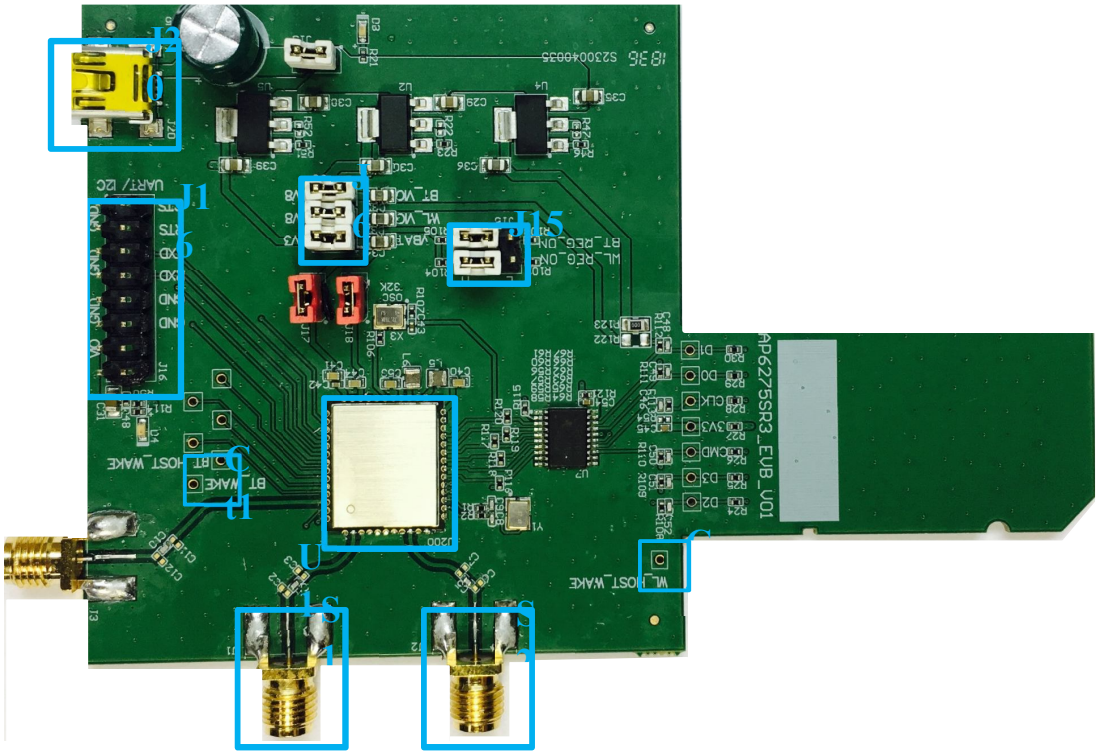

Figure1. Top view of AP6398S2 EVB

Interface highlights:

1. U1: AP6398S2 SIP module.
2. J16: UART interface connects with UART transport board for BT measuring
3. J15: Enable(H) or disable(L) Bluetooth, Wi-Fi function
4. J6: VBAT / WL_VIO / BT_VIO for main system I/O power path.
5. J20: 5V DC mini USB input connector.
6. J8: Standard SDIO interfaces for Wi-Fi performance measured.
7. J1: SMA connector let RF ANT1 signal in/out path, you could connect with RF cable or Dipole antenna.
8. J2, J3: No need connection.
9. Ct1: WLAN and BT control pins, strongly recommended WL_HWAKE(IRQ) connected to MCU.

2. WiFi Function Verification Step

2.1 WiFi SDIO

Using external pull up resistors depends on the SDIO supply voltage. The resistance range is 30 KΩ~40 KΩ on the four data lines and the CMD line as the following circuitry.

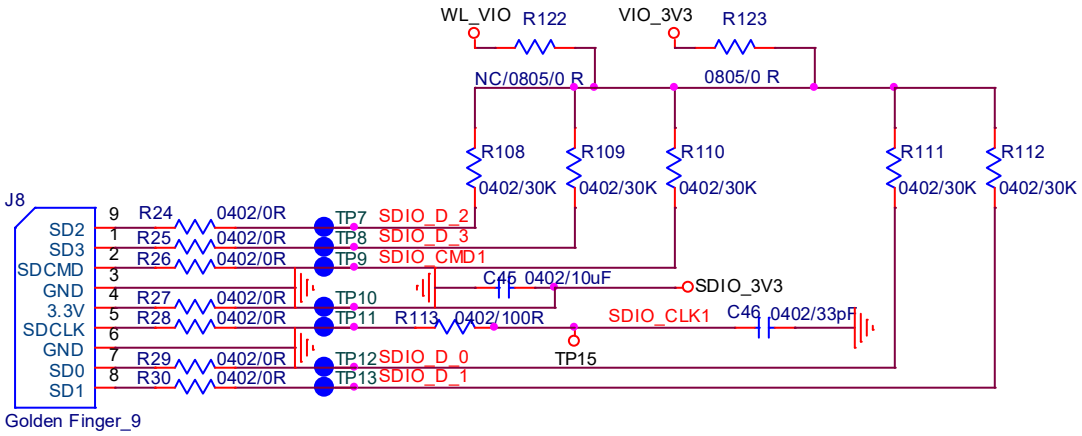

Figure2. WiFi verification connection interface to Host SDIO as using SDIO2.0

Figure3. EVB interface to HOST SDIO 2.0.

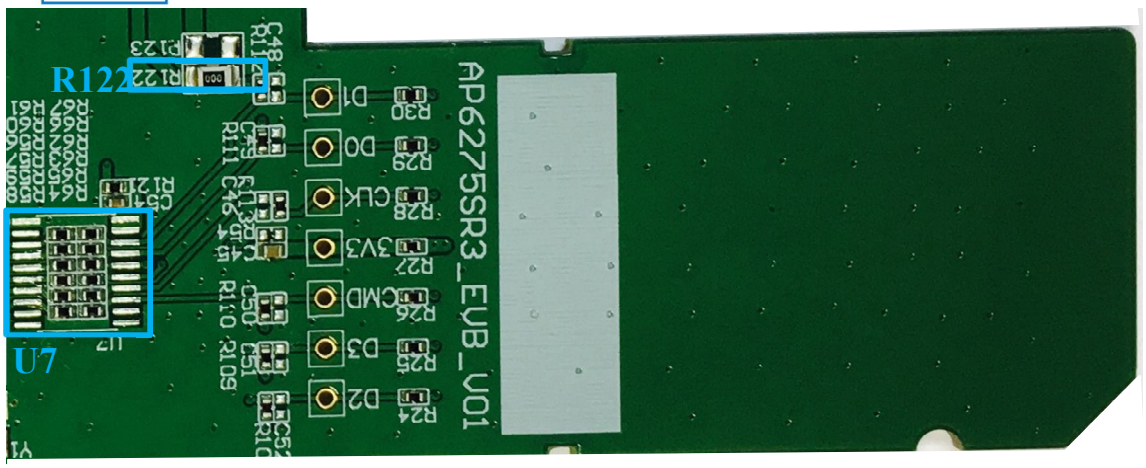

Figure4. EVB interface to HOST SDIO 3.0.

SDIO 2.0 Hardware Setup:

- ✧ Pull up voltage should be 3.3V, so make sure R123 is existed.

SDIO 3.0 Hardware Setup:

- ✧ Pull up voltage should be 1.8V, so make sure R122 is existed.
- ✧ C48/49/46/50/51/52, remove it.

2.2 Hardware Setup

- Refer to Figure2 SDIO pin definition connects the J8 interface of AP6398S2 evaluation board to Host SDIO control interface.
- Using pull high resistors (R108, R109, R110, R111, R112) that resistance is 30Kohm for 1.8V or 3.3V VDDIO pull up voltage. (Pull high resistors are un-necessary if at verification phase.)
- Connects an external antenna at SMA connector on the evaluation board.
- Note to the VDDIO voltage level should be the same with GPIO voltage level of Host CPU. (U7 is voltage level shift to 3.3V.)

2.3 Wi-Fi Software Setup

- Please follow up software guideline of Ampak official released.

3. Bluetooth Function Verification Step

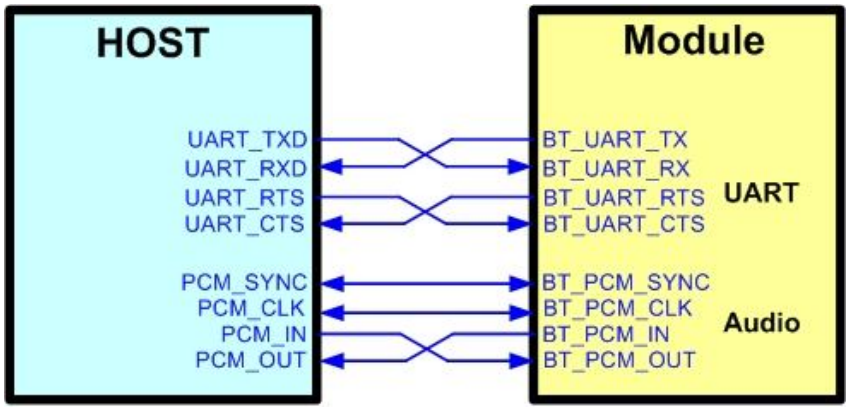

Figure5. Bluetooth verification connection interface to Host UART

Hardware Setup:

- ❖ Refer to Figure5 UART pin definition connects the J16 interface of AP6398S2 evaluation board to Host UART control interface.
- ❖ Connects an external antenna at SMA connector on the evaluation board.
- ❖ Note to the VDDIO voltage level should be the same as GPIO voltage level of Host CPU.

Wi-Fi and Bluetooth software setup:

- ❖ Please follow up software guideline of Ampak official released.